AMENDMENTS TO THE CLAIMS:

Please amend claims 1-11 and add new claims 12-16, as denoted in the following listing. This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended) A circuit designing apparatus comprising:

a logic verification unit configured to perform a logic verification by using a circuit description defining a structure and a specification of a circuit to be designed and a plurality of test vectors;

a profile information generating unit configured to store information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification in every test vector as a profile information;

a logic cone specifying unit configured to specify ~~unit for specifying the~~ changed ~~points~~ logic cones of a changed ~~the~~ circuit description automatically ~~in predetermined unit~~; and

a test vector classifying unit configured to classify ~~classifying~~ the ~~plural~~ test vectors into test vectors ~~those~~ related to ~~with~~ the changed logic cones ~~points~~ and ~~others not~~ test vectors unrelated to the changed logic cones by using the profile information.

2. (Currently amended) ~~A~~ The circuit designing apparatus of claim 1, further comprising:

a logic cone dividing unit configured to divide the ~~for dividing a first~~ circuit description ~~defining the structure and specification of the circuit to be designed in predetermined units~~ into the logic cones;

~~logic verification unit for verifying the logic by using said first circuit description and test vectors;~~

~~profile information generating unit for storing the information about the predetermined unit in the first circuit description to be activated by the test vector during said logic verification in every test vector as profile information;~~

a circuit changing unit configured to change the ~~for changing said first~~ circuit description and to generate a changed ~~generating a second~~ circuit description; and

a formal verification unit configured to verify logic ~~for verifying~~ by formal technology using the circuit description and the changed ~~said first and second~~ circuit description[[s;]]

~~specifying unit for specifying the changed predetermined unit relating to the change in said second circuit description on the basis of the result of said formal verification; and~~

~~test vector classifying unit for classifying the test vectors into those activating the changed predetermined unit and others not by using said profile information~~.

3. (Currently amended) A circuit designing method comprising ~~the steps of~~:

performing a logic verification by using a circuit description defining a structure and a specification of a circuit to be designed and a plurality of test vectors;

storing information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification in every test vector as profile information;

specifying ~~the~~ changed logic cones ~~points~~ of a changed ~~the~~ circuit description automatically ~~in predetermined unit~~; and

classifying the ~~plural~~ test vectors into test vectors ~~those~~ related to ~~with~~ the changed logic cones ~~points~~ and test vectors unrelated to the changed logic cones by using the profile information ~~others not, wherein the second and subsequent logic verification processes are executed by using only the test vectors relating to the changed points~~.

4. (Currently amended) ~~A~~ The circuit designing method of claim 3, further comprising ~~the steps of~~:

~~entering a first circuit description defining the structure and specification of the circuit to be designed;~~

dividing the ~~a first~~ circuit description ~~in predetermined units~~ into the logic cones;

~~verifying the logic by using said first circuit description and test vectors;~~

~~storing the information about the predetermined unit in the first circuit description to be activated by the test vector during said logic verification in every test vector as profile information;~~

changing the ~~said first~~ circuit description and generating the changed ~~a second~~ circuit description; and

verifying logic by formal technology using the circuit description and the changed ~~said first and second~~ circuit description[[s;]]

~~specifying the changed predetermined unit relating to the change in said second circuit description on the basis of the result of said formal verification; and~~

~~classifying the test vectors into those activating the changed predetermined unit and others not by using said profile information~~.

5. (Currently amended) The circuit designing method of claim [[4]]3, wherein the logic verification of the changed ~~second~~ circuit description is executed by using preferentially the test vectors relating to ~~vector for activating~~ the changed ~~predetermined unit~~ logic cones.

6. (Currently amended) The circuit designing method of claim 4, further comprising ~~the step of:~~ issuing a circuit description and processing circuit manufacture by using the ~~said~~ circuit description.

7. (Currently amended) The circuit designing method of claim 5, further comprising ~~the step of:~~ issuing a circuit description and processing circuit design and manufacture by using the ~~said~~ circuit description.

8. (Currently amended) A computer-readable recording medium storing a circuit designing program comprising and making a ~~the~~ computer execute ~~the processes of~~:

~~dividing process for dividing a first circuit description defining the structure and specification of the circuit to be designed in predetermined units;~~

instructions configured to perform ~~logic verification process for verifying~~ a logic verification by using a ~~the first~~ circuit description defining a structure and a specification of a circuit to be designed and a plurality of test vectors;

instructions configured to store ~~profile information generating process for storing the~~ information about a plurality of logic cones ~~the predetermined unit~~ in the ~~first~~ circuit description to be activated by the test vectors during the logic verification in every test vector as profile information;

~~circuit changing process for changing the first circuit description and generating a second circuit description, formal verification process for verifying by formal technology using said first and second circuit descriptions;~~

instructions configured to specify ~~specifying process for specifying the~~ changed ~~predetermined unit relating to the change in the second~~ logic cones of a changed circuit description automatically ~~on the basis of the result of formal verification~~; and

instructions configured to classify ~~test vector classifying process for classifying~~ the test vectors into test vectors related to logic cones ~~those activating~~ the changed ~~predetermined unit~~ and test vectors unrelated to the changed logic cones ~~others not~~ by using the profile information.

9. (Currently amended) The computer-readable recording medium storing a circuit designing program of claim 8, wherein the logic verification of the changed ~~second~~ circuit description is executed by using preferentially the test vectors relating to ~~vector for activating~~ the changed ~~predetermined unit~~ logic cones.

10. (Currently amended) The computer-readable recording medium storing a circuit designing program of claim 8, further comprising and making the computer execute ~~the process of~~:

instructions configured to output ~~process of~~ a circuit description,

wherein circuit manufacture is processed by using the ~~said~~ circuit description.

11. (Currently amended) The computer-readable recording medium storing a circuit designing program of claim ~~9~~ 8, further comprising and making the computer execute ~~the process of~~:

~~output process of a circuit description,~~

~~wherein circuit manufacture is processed by using said circuit description~~

instructions configured to divide the circuit description into the logic cones;

instructions configured to change the circuit description and for generating the changed circuit description; and

instructions configured to verify by formal technology using the circuit description and the changed circuit description.

12. (New) The circuit designing apparatus of claim 1, wherein the logic verification of the changed circuit description is executed by using preferentially the test vectors relating to the changed logic cones.

13. (New) The circuit designing apparatus of claim 1, wherein the second and subsequent logic verifications are executed by using only the test vectors relating to the changed logic cones.

14. (New) The circuit designing apparatus of claim 2, wherein the logic cone specifying unit specifies the changed logic cones on the basis of a result of the formal verification.

15. (New) The circuit designing method of claim 3, wherein the second and subsequent logic verifications are executed by using only the test vectors relating to the changed logic cones.

16. (New) The computer-readable recording medium storing a circuit designing program of claim 8, wherein the second and subsequent logic verifications are executed by using only the test vectors relating to the changed logic cones.